CLAIMS

1. A method of determining the value of a signal, in which N previously detected bits (where N is at least 2) of a demodulated bit stream are used to select which one of a plurality of threshold levels against which the current demodulated bit is to be compared in a bit slicer and is to be updated using the current demodulated bit.

2. A method as claimed in claim 1, characterised by having a plurality of threshold levels and having P (where P is at least 2) mean estimators associated with each of the threshold levels, and for a selected one of the threshold levels obtaining the average value of the associated P mean estimators and using the result as the current selected one of the threshold values.

3. A method as claimed in claim 1, characterised by intermittently integrating the demodulated bit stream over at least 2 bit periods and comparing the result with the selected threshold value and using the result to update the selected threshold value.

4. A method as claimed in claim 3, characterised by oversampling the demodulated bit stream by a factor M, where M is an integer of the order of 20, and intermittently integrating at least one sample in the vicinity of the M/2 sample of each of the at least 2 bit periods to generate the demodulated signal to be compared with the selected one of the threshold values.

5. A method as claimed in claim 3, characterised by selecting at least 2 samples from the more recent bit period and at least one sample from the preceding bit period.

6. A method as claimed in Claim 3, characterised by oversampling the demodulated bit stream, weighting the samples, and integrating the

weighted samples to generate the demodulated signal to be compared with the selected one of the threshold values.

7. A method as claimed in claim 1, characterised by selecting one of a plurality of preset default threshold values in accordance with a bit sequence formed by the N previously detected bits and the latest detected bit as determined by the bit slicer, obtaining a demodulated signal integrated over at least 2 bit periods, subtracting the demodulated signal from the selected preset default value to produce a dc offset estimate, deriving a mean dc offset estimate from the current dc offset estimate and a plurality of preceding dc offset estimates, combining the mean dc offset estimate with a selected threshold value and applying the combined signal to a threshold input of the bit slicer.

8. A method as claimed in claim 7, characterised by subtracting the dc offset estimate from the demodulated signal prior to updating the selected threshold value.

9. A method as claimed in Claim 7, characterised by adjusting the responsiveness of the mean dc offset estimate with respect to drifts.

10. A method of effecting dc offset compensation in a receiver having a variable threshold bit slicer, comprising selecting one of a plurality of preset default n bit values in accordance with a bit sequence formed by the latest and (n – 1) earlier bit values as determined by the bit slicer, obtaining a demodulated signal integrated over at least 2 bit periods, subtracting the demodulated signal from the selected preset default value to produce a dc offset estimate, deriving a mean dc offset estimate from the current dc offset estimate and a plurality of preceding dc offset estimates, and using the mean dc offset estimate to remove the effects of dc offset in determining the value of a demodulated signal.

11. A method as claimed in Claim 10, characterised in that the mean dc offset estimate is combined with a selected threshold value and in that the combined signal is applied to a threshold input of the bit slicer.

12. A method as claimed in Claim 10, characterised by adjusting the responsiveness of the mean dc offset estimate with respect to drift.

13. A receiver having a variable threshold slicer, comprising means for deriving a demodulated bit rate signal, means for storing a plurality of threshold values, each of the threshold values being selectively adjustable, means for selecting the threshold value for comparison with the current bit and for adjustment in response to a sequence of N bits (where N is at least 2) received prior to the current bit and means for using the current bit to update the selected threshold value.

14. A receiver as claimed in claim 13, characterised in that the means for deriving a demodulated bit rate signal includes a non-continuous integrate and dump stage for integrating the demodulated signal over a predetermined number of bit rate periods and supplying the result to the bit slicer and to the means for updating the selected threshold value.

15. A receiver as claimed in claim 13, characterised by means for oversampling the demodulated bit stream by a factor M, where M is an integer of the order of 20, and means for intermittently integrating at least one sample in the vicinity of the M/2 sample of each of at least 2 of the predetermined number of bit rate periods to generate the demodulated signal to be compared with the selected one of the threshold values.

16. A receiver as claimed in Claim 13, characterised by means for oversampling the demodulated bit stream, means for weighting the samples obtained, and integrating means for integrating the weighted samples to

generate the demodulated signal to be compared with the selected one of the threshold values.

17. A receiver as claimed in claim 13, characterised by means for selecting one of a plurality of preset default threshold values in accordance with a bit sequence formed by the N previously detected bits and the latest detected bit as determined by the bit slicer, means for obtaining a demodulated signal integrated over at least 2 bit periods, means for subtracting the demodulated signal from the selected preset default value to produce a dc offset estimate, means for deriving a mean dc offset estimate from the current dc offset estimate and a plurality of preceding dc offset estimates, and means for combining the mean dc offset estimate with a selected threshold value and for applying the combined signal to a threshold input of the bit slicer.

18. A receiver as claimed in Claim 17, characterised by means for adjusting the responsiveness of the mean dc offset estimate with respect to drift.